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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,484	08/05/2003	Tu-Anh Tran	SC12598TK	6798

23125 7590 02/01/2005

FREESCALE SEMICONDUCTOR, INC.  
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EXAMINER
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NGUYEN, VINH P

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/634,484	<b>Applicant(s)</b> TRAN ET AL	
	<b>Examiner</b> VINH P NGUYEN	<b>Art Unit</b> 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 August 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☒ Claim(s) 1-38 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 August 2003 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>0803</u> . | 6) <input type="checkbox"/> Other: _____  |

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature of “a functional block of active circuitry” as recited in claim 1, the feature of “logic of a system on chip (SOC)” as recited in claims 19 and 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The disclosure is objected to because of the following informalities: it appears that the specification does not have description for “a functional block of active circuitry”, “a design for test (DFT) design of hardware and software “, “a metal layer pad on a periphery region of the die”, “an area of I/O cells”.

Appropriate correction is required.

3. Claims 1-38 are objected to because of the following informalities: In claims 1,26 and 36, it is unclear what “a functional block of active circuitry” represents. Is it referred to “module (12)” or “transistor level (27)” or “driver (47)” or a combination of both?

In claim 3, it is unclear what “metal layer pads” represent. Are they shown in any of drawings? Are they the same as “test pad (34)” or are they different from the test pad (34).

In claim 5, it is unclear what “an underlying passivation layer” represents. Is it shown in any of drawings?

In claim 14, it is unclear what “a design for test (DFT) design of hardware and software “ represents. Is it shown in any of drawings?

In claim 16, it is unclear what “a metal layer pad on a periphery region of the die” represents. Is it shown in any of drawings?

In claim 18, it is unclear what “an area of I/O cells” and “metal layer pads on a periphery of the die” represent. Are they shown in any of drawings?

In claims 32-33, it is unclear what “functional block of the integrated circuit” represent. Is it shown in any of drawings? Is it different from functional block of circuitry” or is it the same as “functional block of circuitry”. Is it referred to “module (12)”, “transistor level (27) “ or “driver (47)” or a combination of both?

In claim 37, it is unclear what “functional block of active circuitry” represents. Is it referred to “module (12)”, “transistor level (27)” or “driver (47)” or a combination of both?

In claim 38, it is unclear what “a metal layer pad on a periphery region of the die” represents. Is it shown in any of drawings?

The dependent claims not specifically address share the same objection as they depend from objected base claims.

Appropriate correction is required.

4. Claims 1-38 would be allowable if the correction overcomes the objections because the prior art does not disclose a test pad structure in a center region of the die wherein the first portion of the test structure is not overlaying the passivation layer and a second portion is overlaying the passivation layer.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kasai (Pat # 6,008,061) disclose method of manufacturing semiconductor device having a test pad.

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Hsuan et al (Pat # 6,214,630) disclose wafer level integrated circuit structure and method of manufacturing the same.


6. This application is in condition for allowance except for the following formal matters as mentioned in paragraphs 1-3.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P NGUYEN whose telephone number is (571)-272-1964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
VINH P. NGUYEN  
PRIMARY EXAMINER  
ART UNIT 2829  
01/27/05